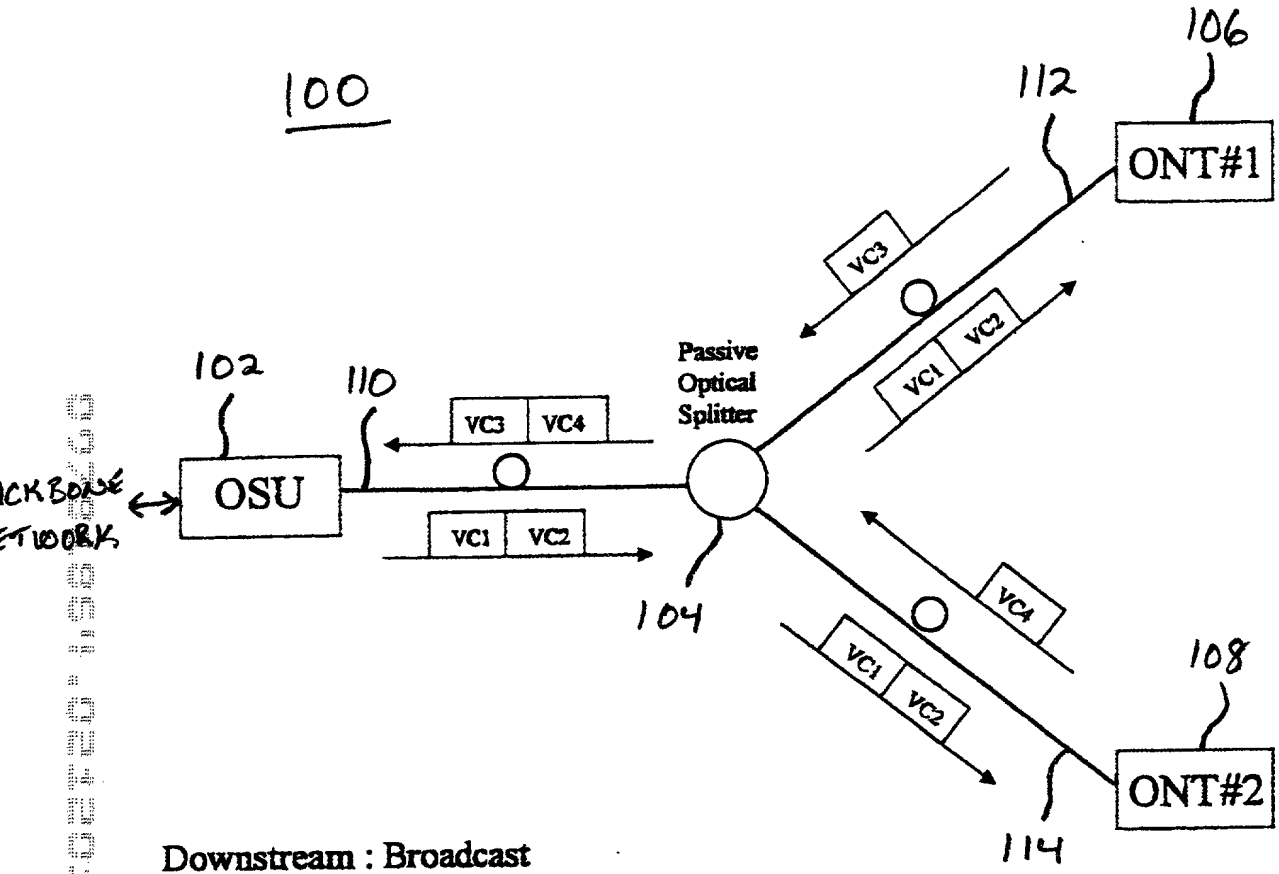
FIG. 1 (PRIOR ART)



Downstream : Broadcast
Upstream : TDMA (Time Division Multiple Access)

FIG. 2 (PRIOR ART)

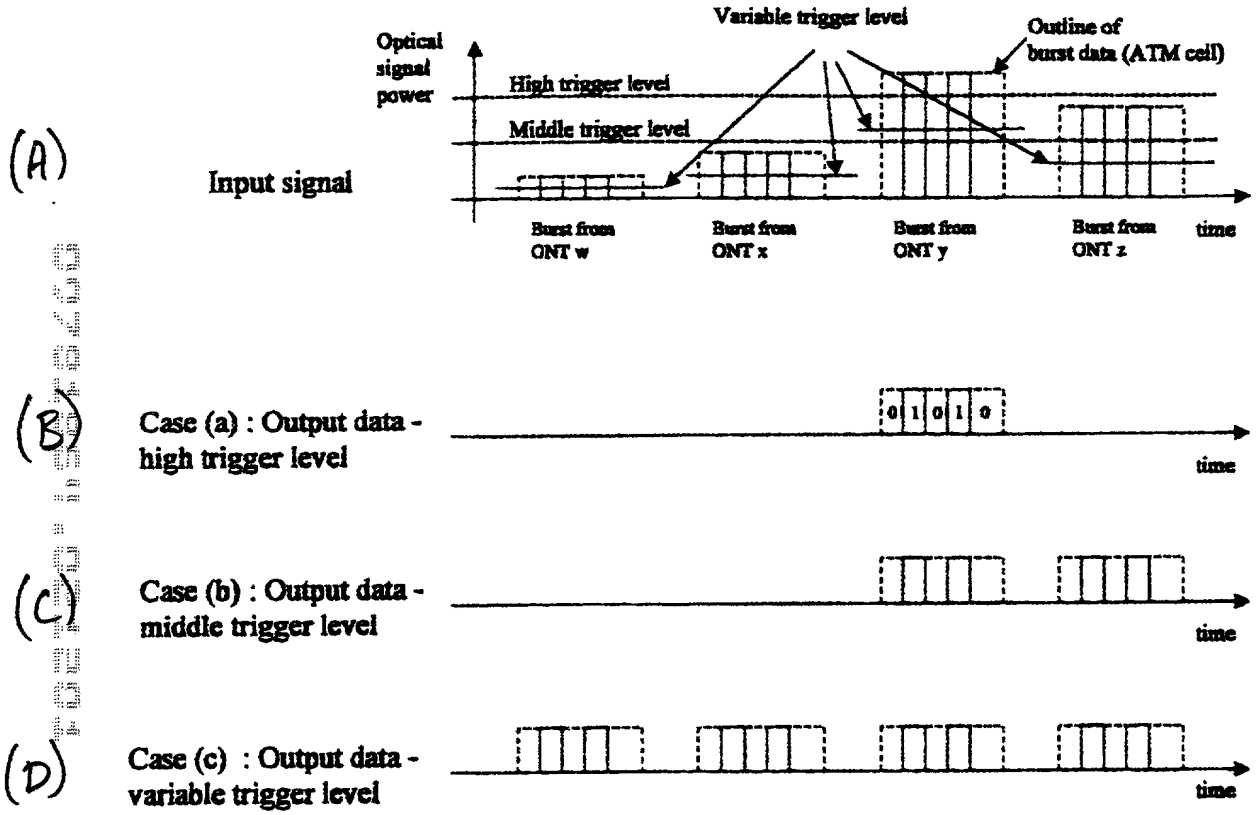


FIG. 3

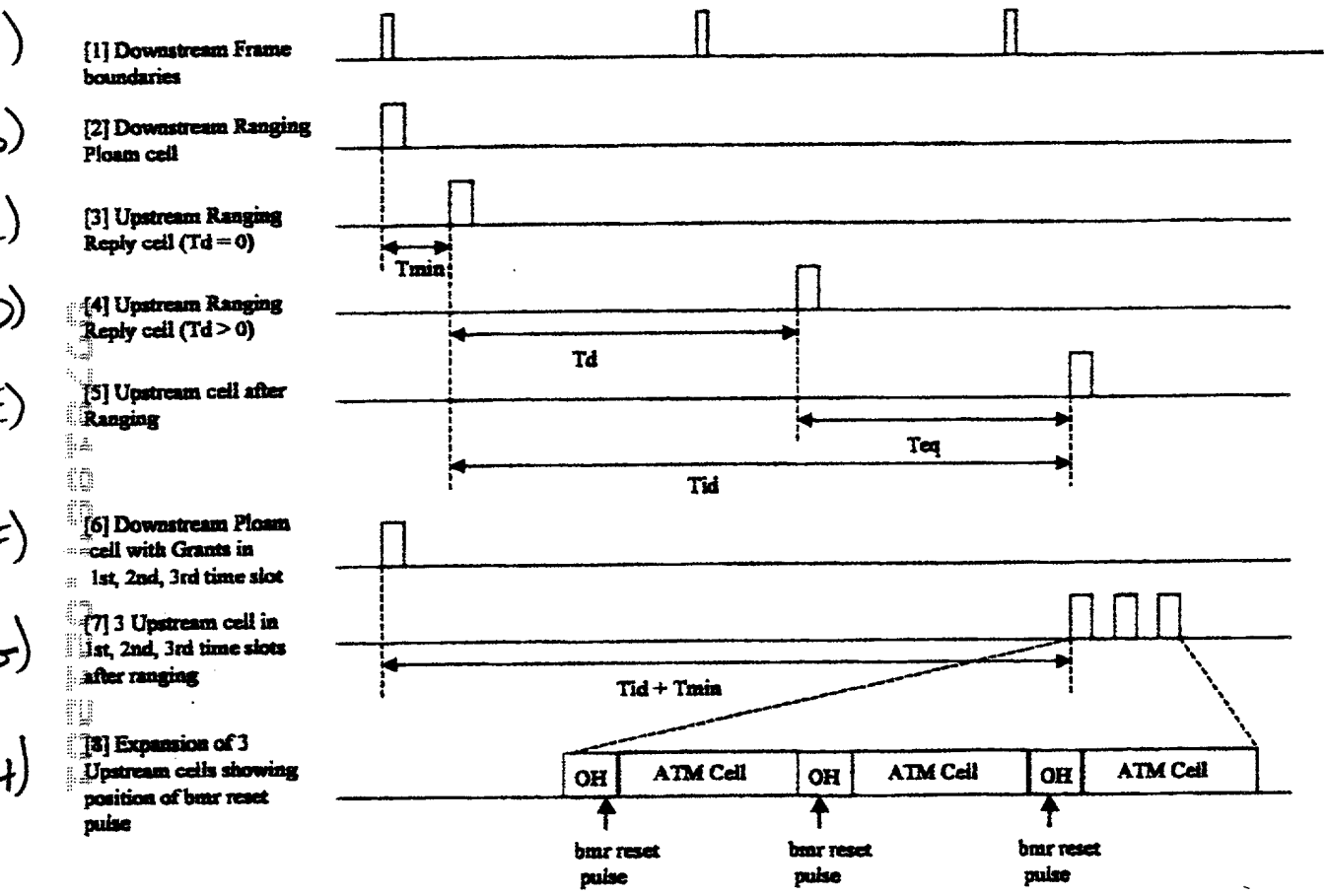
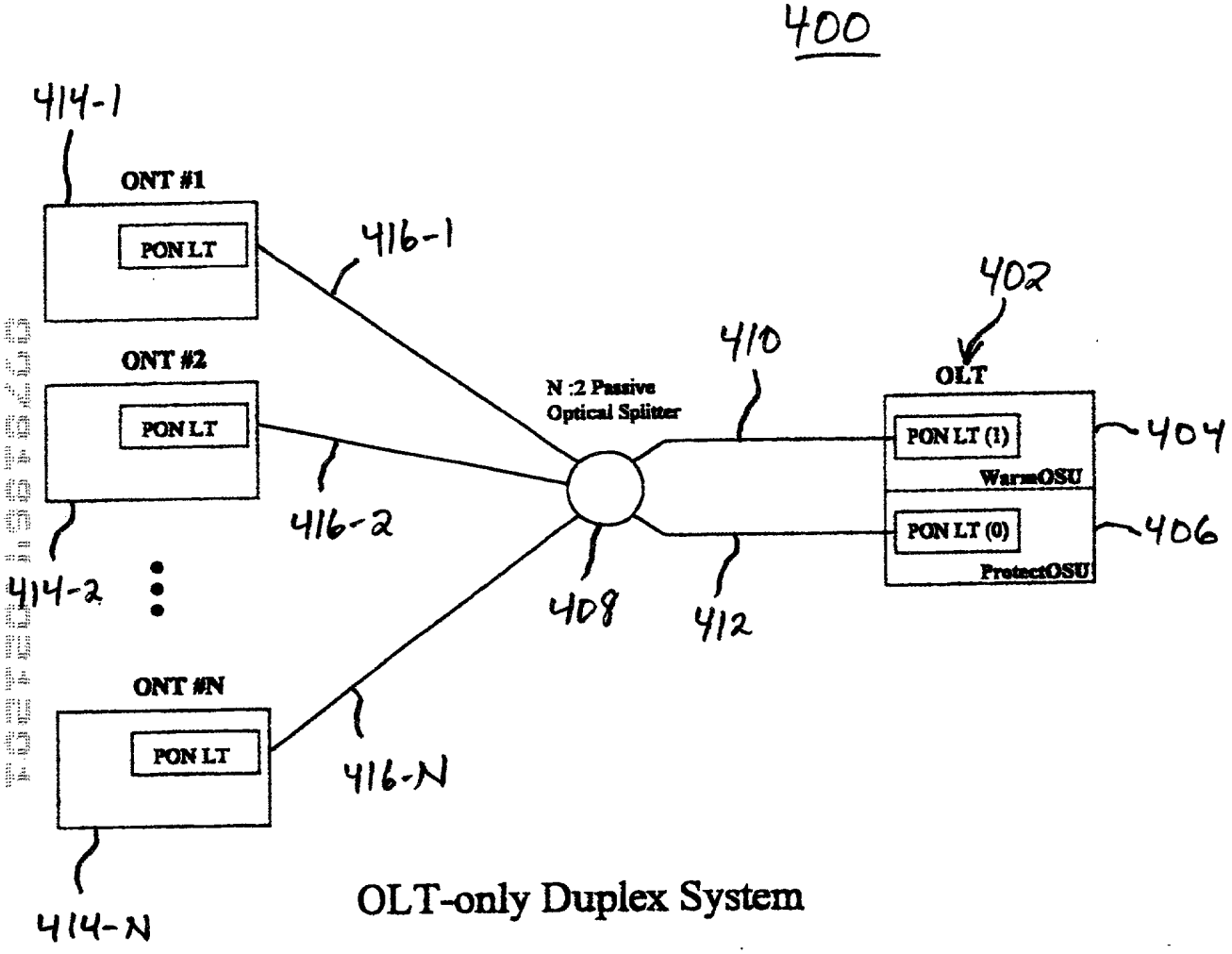
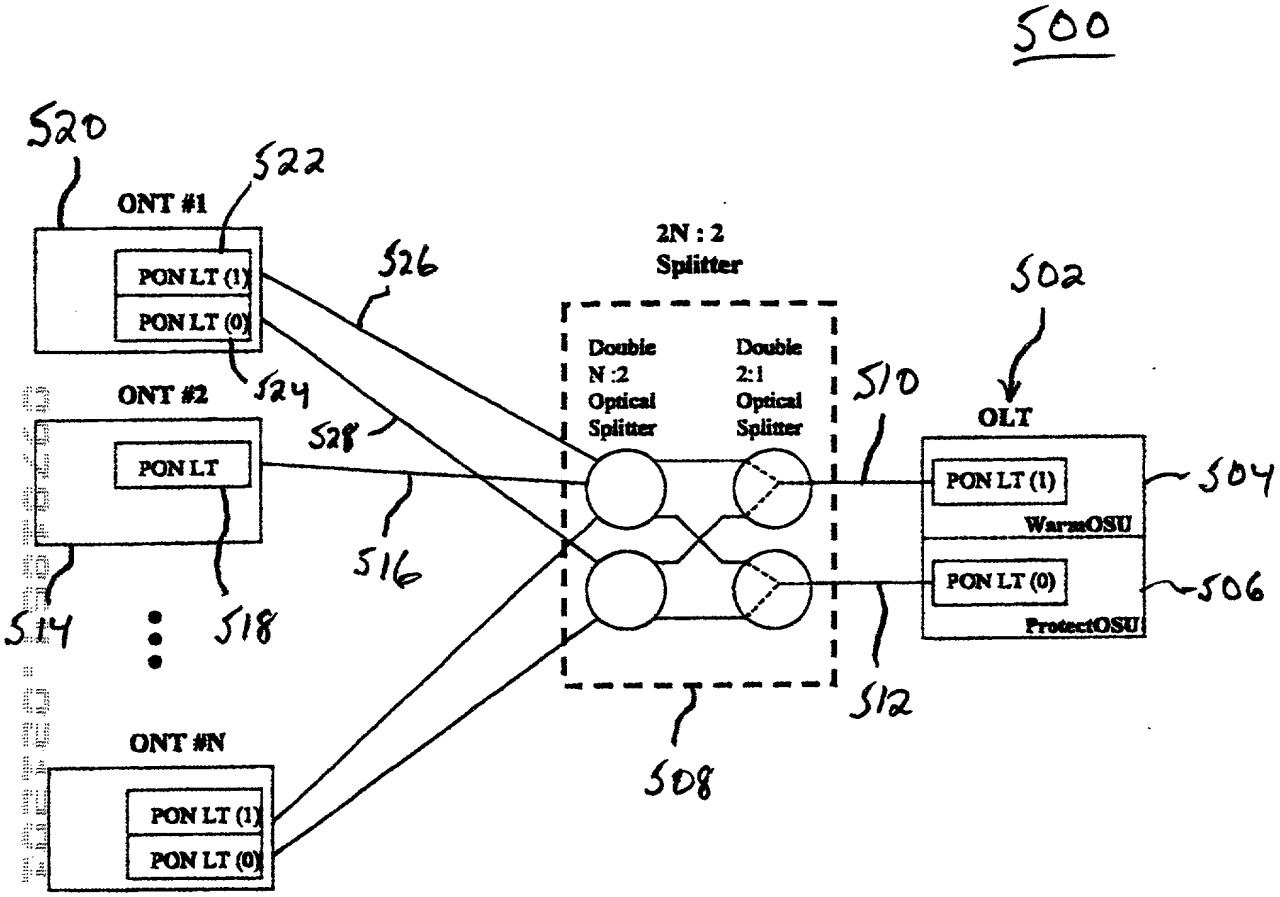

[1] Downstream Frame boundaries
[2] Downstream Ranging Ploam cell
[3] Upstream Ranging Reply cell (Td = 0)
Tmin
[4] Upstream Ranging Reply cell (Td > 0)
Td
[5] Upstream cell after Ranging
Teq
Tid
[6] Downstream Ploam cell with Grants in 1st, 2nd, 3rd time slot
[7] 3 Upstream cell in 1st, 2nd, 3rd time slots after ranging
Tid + Tmin
[8] Expansion of 3 Upstream cells showing position of bmr reset pulse
OH
ATM Cell
OH
ATM Cell
OH
ATM Cell
bmr reset pulse
bmr reset pulse
bmr reset pulse

FIG. 4



OLT-only Duplex System

FIG. 5



Partial Duplex System

FIG. 6

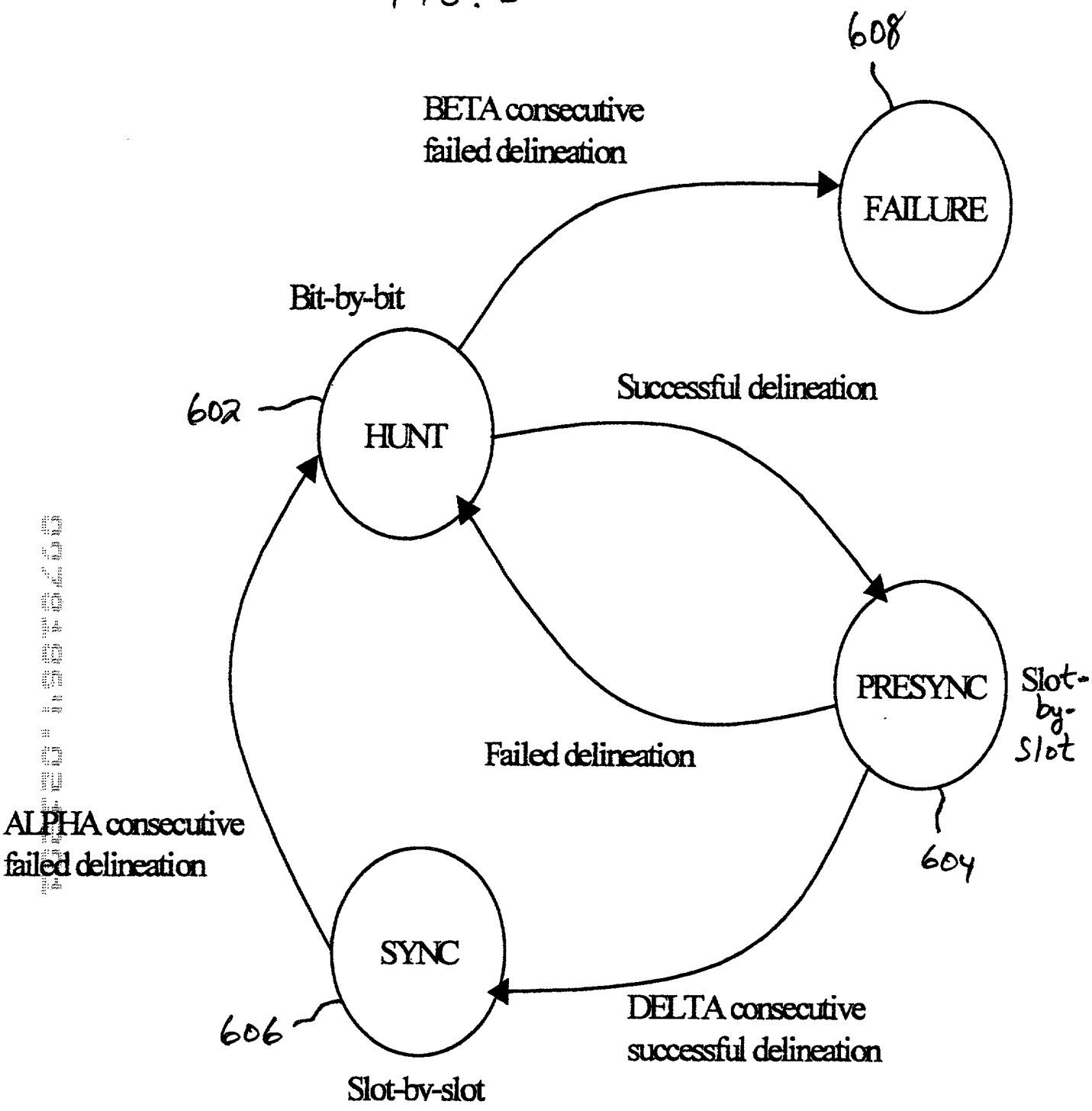

608
BETA consecutive
failed delineation
FAILURE
Bit-by-bit
602
HUNT
Successful delineation
PRESYNC
Slot-
by-
Slot
Failed delineation
ALPHA consecutive
failed delineation
604
SYNC
606
DELTA consecutive
successful delineation
Slot-by-slot

FIG. 7

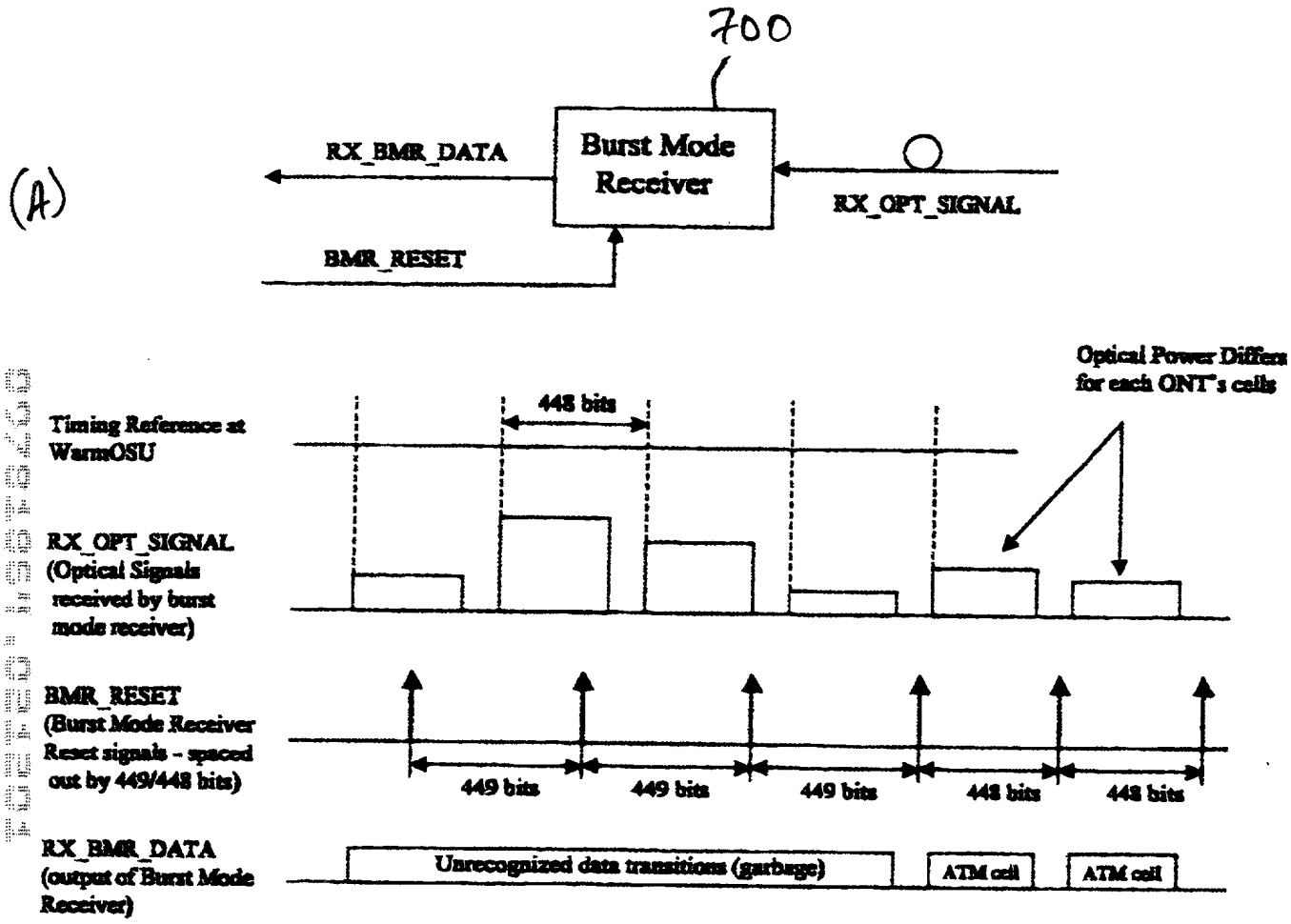

700
(A)
RX_BMR_DATA
Burst Mode Receiver
RX_OPT_SIGNAL
BMR_RESET
Optical Power Differs for each ONT's cells
(B)
Timing Reference at WarmOSU
448 bits
(C)
RX_OPT_SIGNAL (Optical Signals received by burst mode receiver)
(D)
BMR_RESET (Burst Mode Receiver Reset signals - spaced out by 449/448 bits)
449 bits
449 bits
449 bits
448 bits
448 bits
(E)
RX_BMR_DATA (output of Burst Mode Receiver)
Unrecognized data transitions (garbage)
ATM cell
ATM cell

FIG. 8

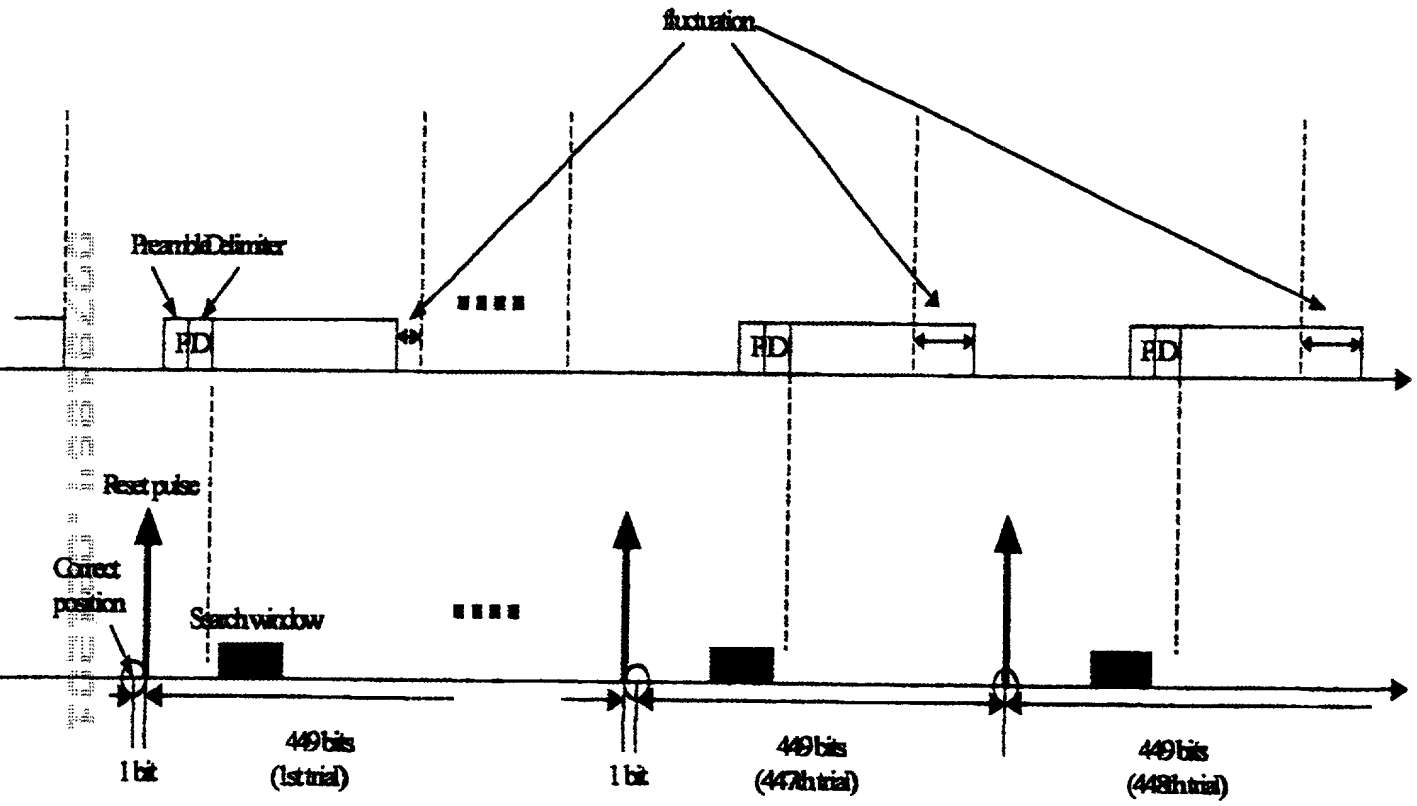
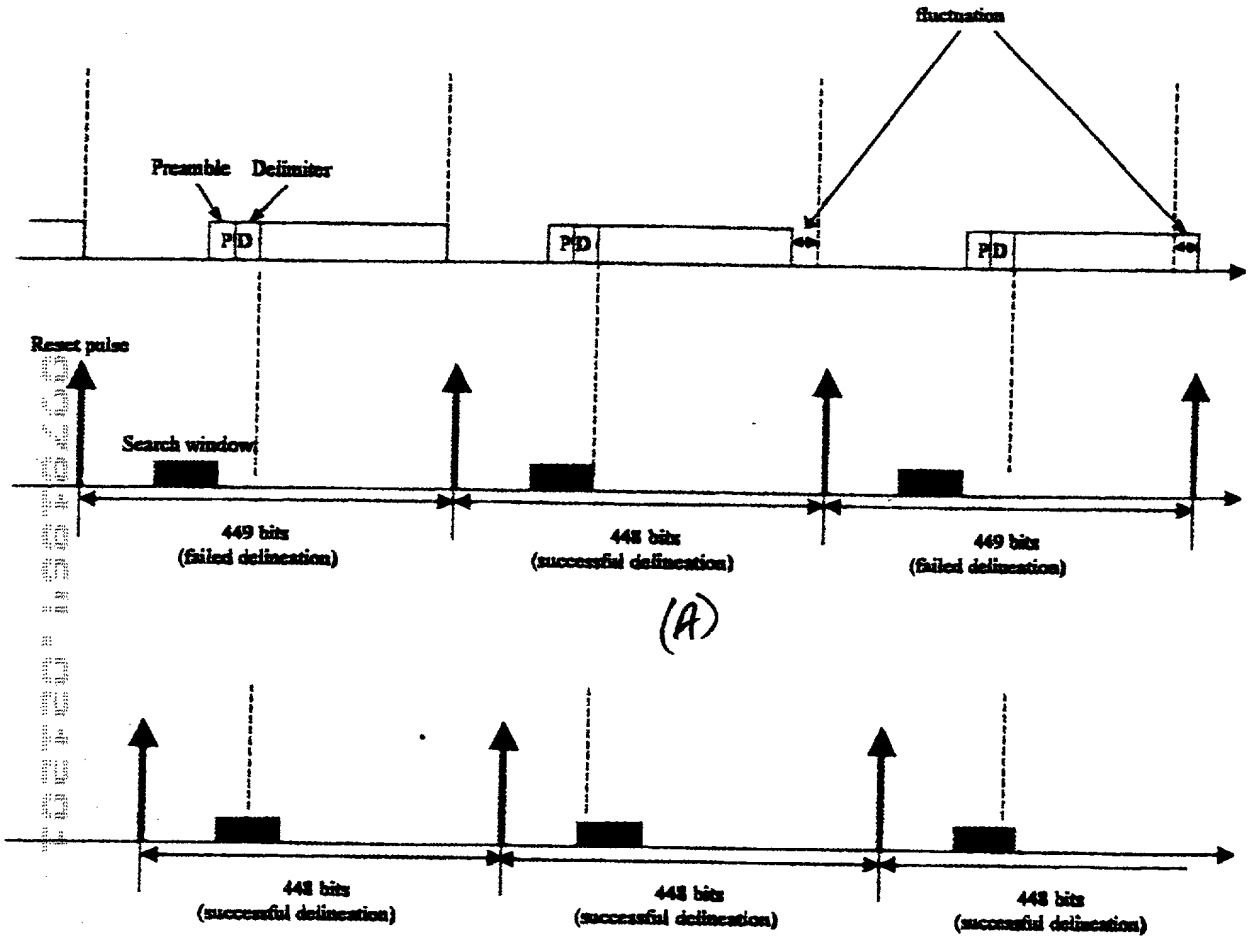

fluctuation
Preamble Delimiter
FD
FD
FD
Reset pulse
Correct position
Search window
1 bit
449 bits
(1st trial)
1 bit
449 bits
(447th trial)
449 bits
(448th trial)

FIG. 9

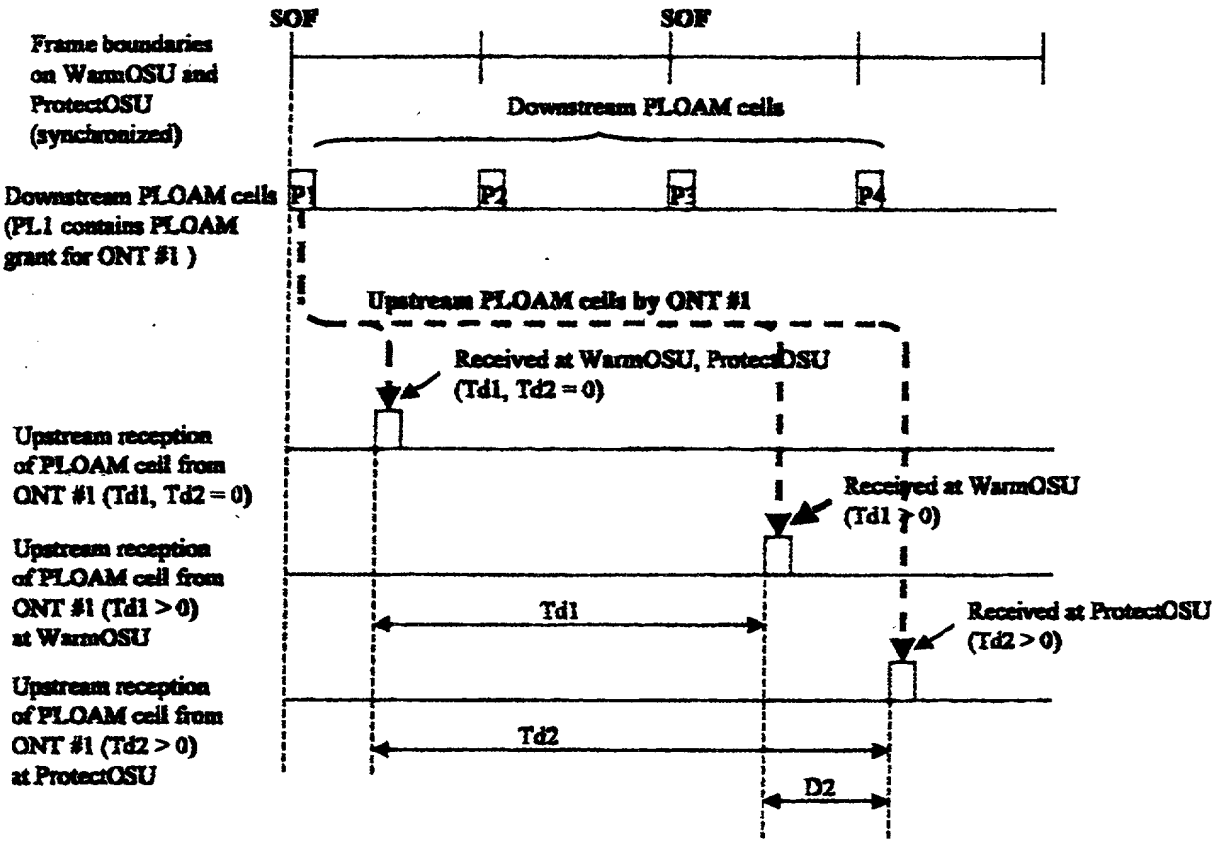

fluctuation
Preamble
Delimiter
PD
PD
PD
Reset pulse
Search window
449 bits
(failed delineation)
448 bits
(successful delineation)
449 bits
(failed delineation)

(A)

448 bits
(successful delineation)
448 bits
(successful delineation)
448 bits
(successful delineation)

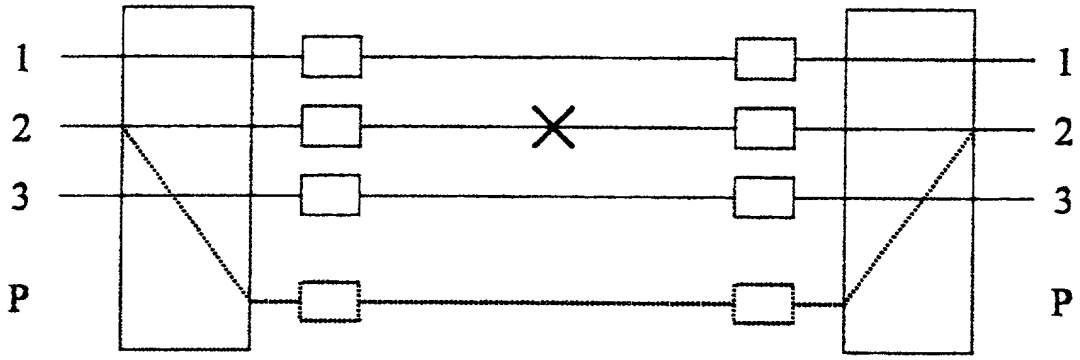
(B)

FIG. 10



Td1 : delay measured at WarmOSU
Td2 : delay measured at ProtectOSU
D2 : time difference between start of frame in WarmOSU and ProtectOSU, due to difference in distance to splitter
*SOF : Start of Frame

FIG. 11



1:N Protection (example N = 3)

FIG. 12

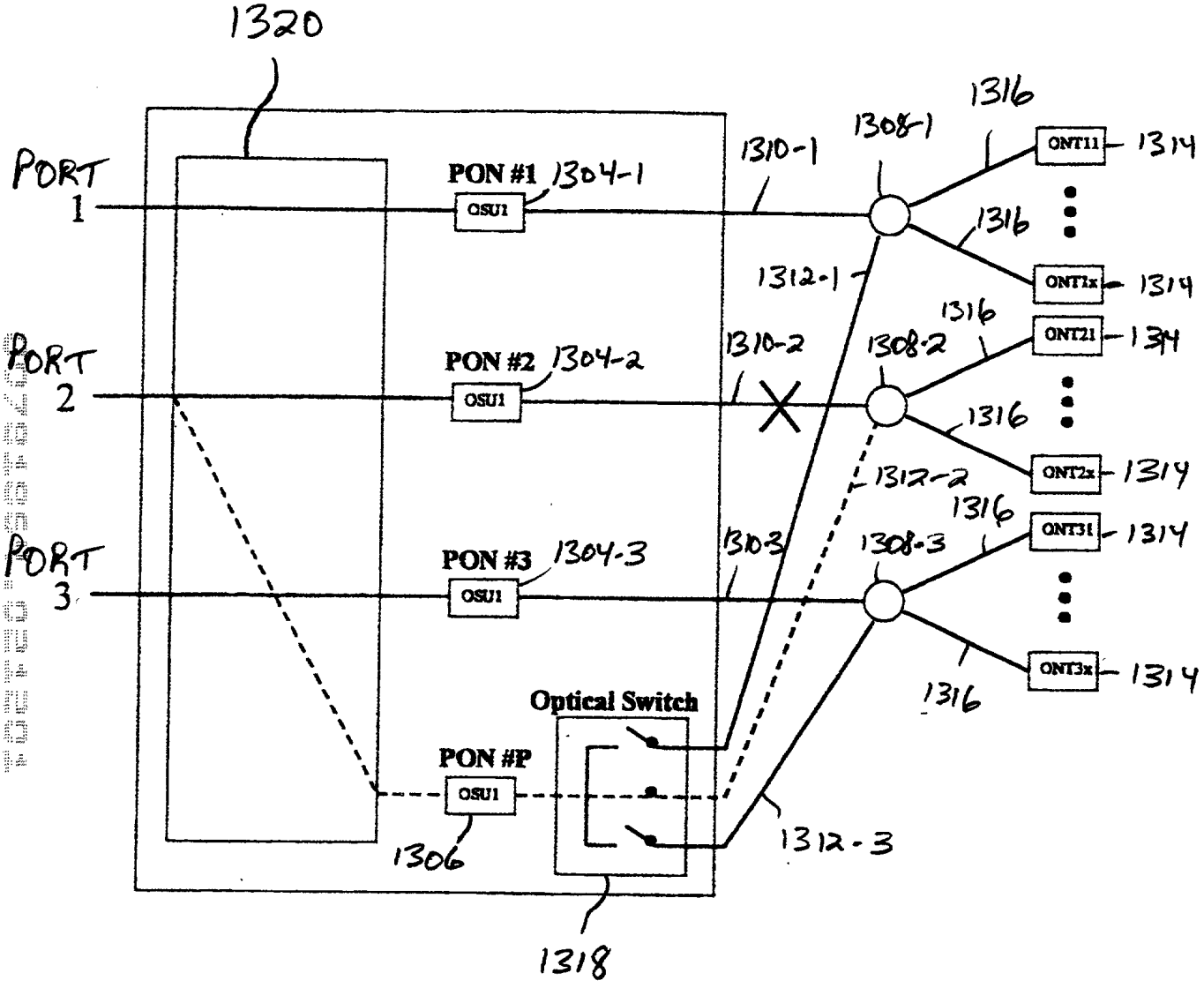
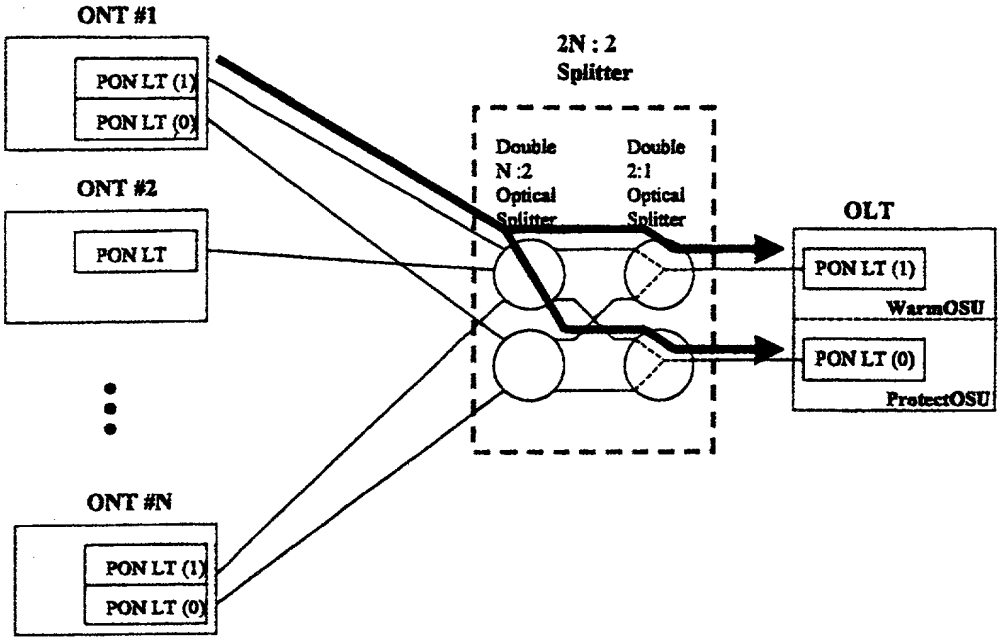
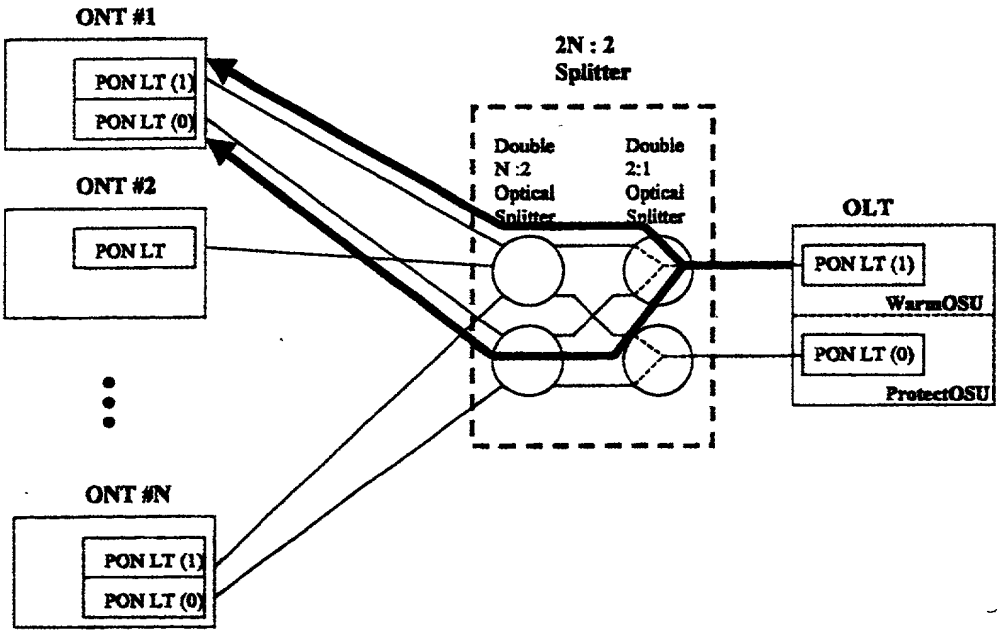

1320
PORT 1
PORT 2
PORT 3
PON #1
1304-1
OSU1
PON #2
1304-2
OSU1
PON #3
1304-3
OSU1
PON #P
OSU1
1306
Optical Switch
1318
1310-1
1310-2
1310-3
1308-1
1308-2
1308-3
1312-1
1312-2
1312-3
1316
ONT11
ONT1x
ONT21
ONT2x
ONT31
ONT3x
1314

FIG. 13



Partial Duplex System

FIG. 14



Partial Duplex System